P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D T_A = 25°C
-25V	40mΩ @ V_{GS} = -4.5V	-5.2 A

Features and Benefits

- Low Q_g & Q_{gd}
- Small Footprint 1.5-mm × 1.5-mm
- **Gate ESD Protection 6kV**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description and Applications

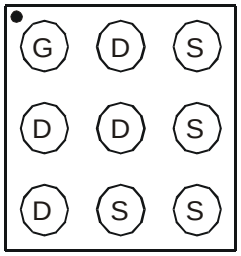
This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Battery Management
- Load Switch
- Battery Protection

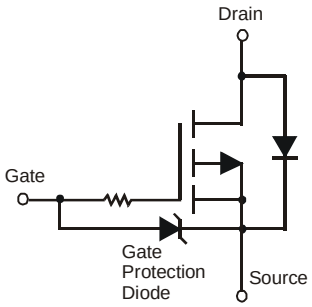
Mechanical Data

- Case: U-WLB1515-9
- Terminal Connections: See Diagram Below
- Weight: 0.0018 grams (approximate)

ESD PROTECTED TO 6kV



Top-View
Pin Configuration



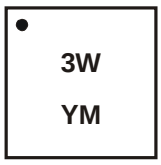
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2540UCB9-7	U-WLB1515-9	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com.

Marking Information



3W = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: Y = 2011)
M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-25	V
Gate-Source Voltage			V_{GSS}	-6	V
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_A = 25 C T_A = 70 C	I_D	-4.0 -3.0	A
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = 25 C T_A = 70 C	I_D	-5.2 -4.0	A
Pulsed Drain Current (Pulse duration 10µs, duty cycle ≤1%)			I_{DM}	-30	A
Continuous Source Pin Current (Note 6)			I_S	-2.0	A
Pulsed Source Pin Current (Pulse duration 10µs, duty cycle ≤1%)			I_{SM}	-15	A
Continuous Gate Clamp Current (Note 5)			I_G	-0.6	A
Pulsed Gate Clamp Current (Pulse duration 10µs, duty cycle ≤1%)			I_{GM}	-8	A

Thermal Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	1.0	W
Total Power Dissipation (Note 6)	P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	126.8	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	69	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-25	-	-	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current @T_C = 25°C	I_{DSS}	-	-	-1	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	-100	nA	V_{GS} = -6V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-0.6	-1.1	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	33	40	mΩ	V_{GS} = -4.5V, I_D = - 2A
			42	50		V_{GS} = -2.5V, I_D = -2A
			52	60		V_{GS} = -1.8V, I_D = -2A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	12	-	S	V_{DS} = -10V, I_D = -2A
Diode Forward Voltage (Note 5)	V_{SD}	-	-0.7	-1	V	V_{GS} = 0V, I_S = -2A
Reverse Recovery Charge	Q_{rr}	-	100	-	nC	V_{dd} = –9.5V, I_F = –2A, di/dt = 200A/µs
Reverse Recovery Time	t_{rr}	-	130	-	ns	
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	342	450	pF	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	174	225	pF	
Reverse Transfer Capacitance	C_{rss}	-	70	90	pF	
Series Gate Resistance	R_G		28	35	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (4.5V)	Q_g	-	4.8	6.0	nC	V_{GS} = -4.5V, V_{DS} = -10V, I_D = -2A
Gate-Source Charge	Q_{gs}	-	0.5	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.0	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	11	-	ns	V_{DD} = -10V, V_{GS} = -4.5V, I_{DS} = -2A, R_G = 2Ω,
Turn-On Rise Time	t_r	-	12	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	56	-	ns	
Turn-Off Fall Time	t_f	-	42	-	ns	

Notes: 5. Device mounted on FR-4 PCB with minimum recommended pad layout.
6. Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

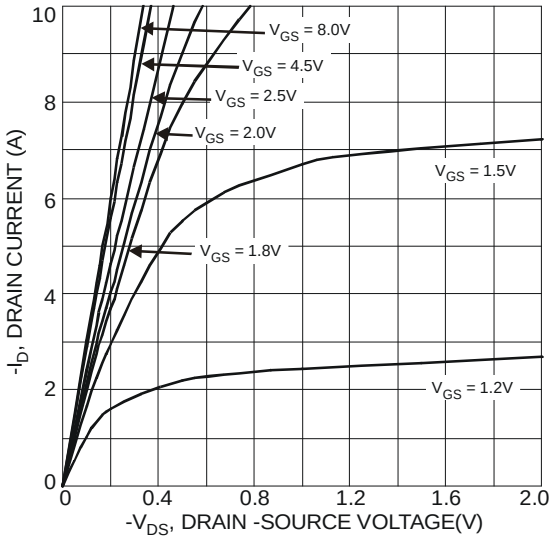


Fig. 1 Typical Output Characteristics

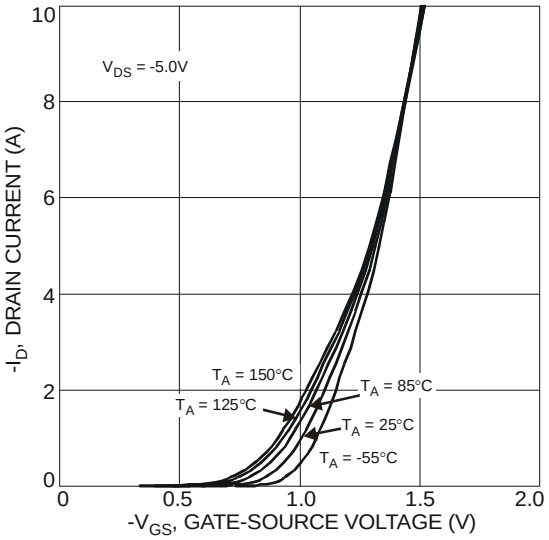


Fig. 2 Typical Transfer Characteristics

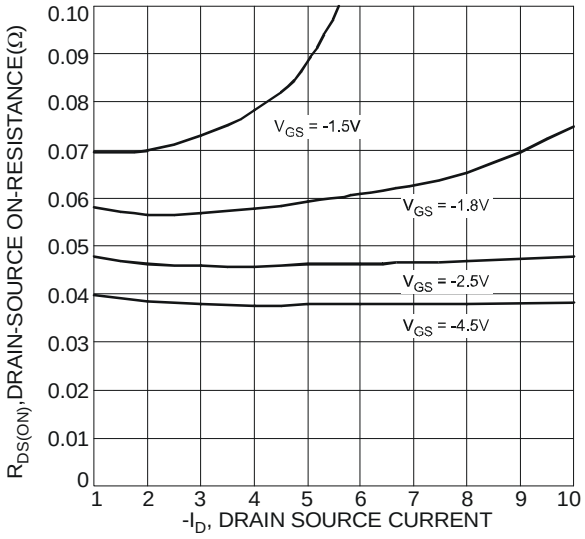


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

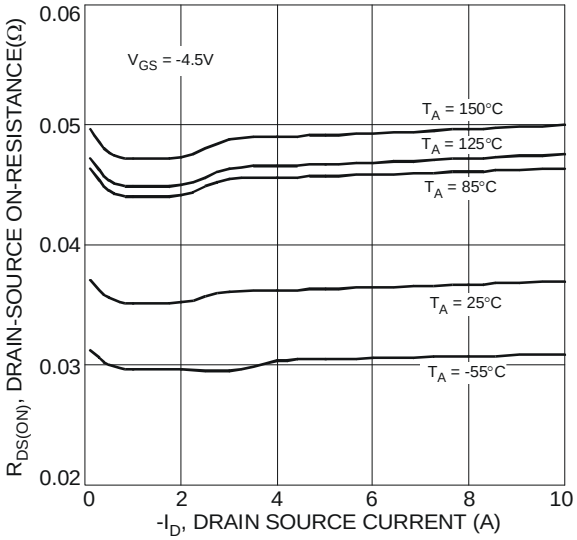


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

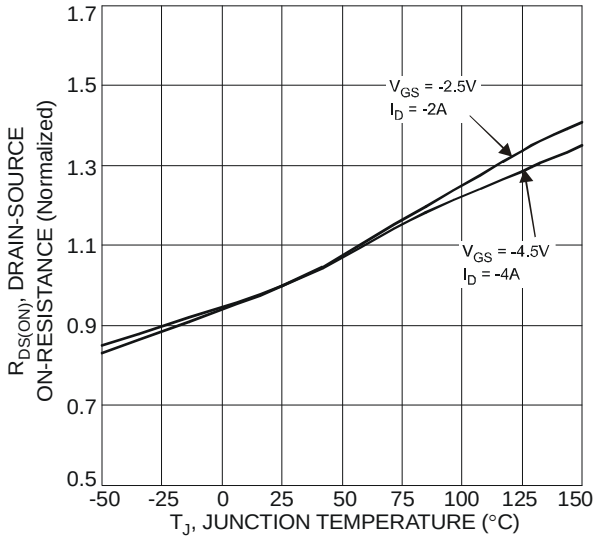


Fig. 5 On-Resistance Variation with Temperature

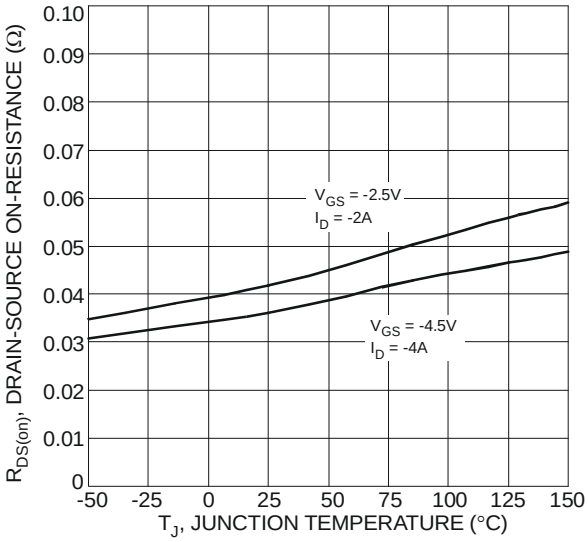


Fig. 6 On-Resistance Variation with Temperature

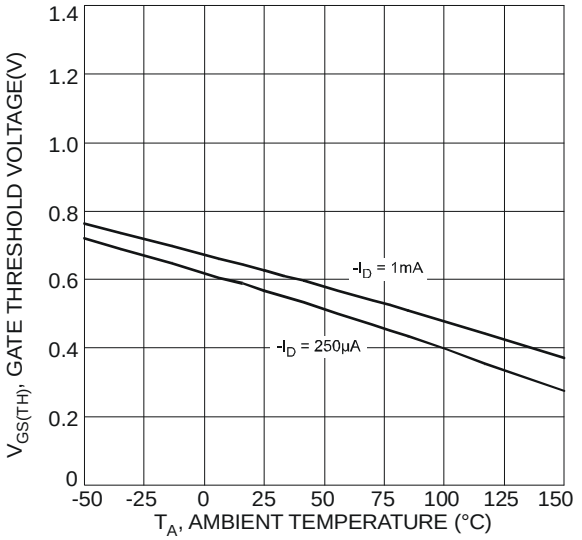


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

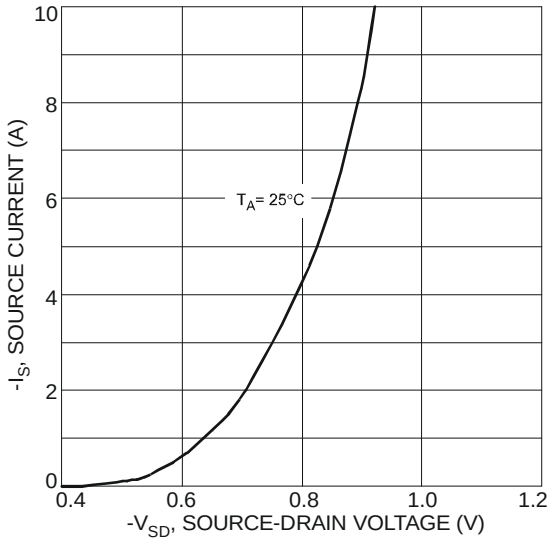


Fig. 8 Diode Forward Voltage vs. Current

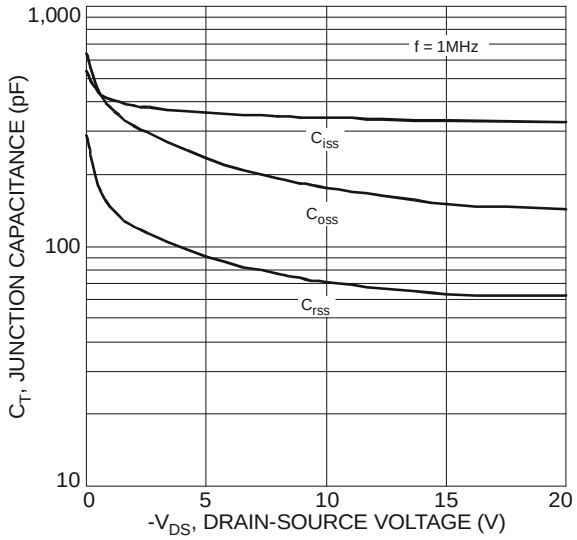


Fig. 9 Typical Junction Capacitance

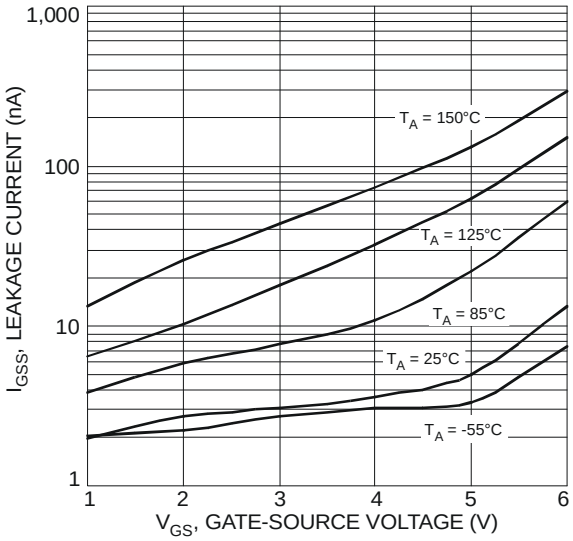


Fig. 10 Gate-Source Leakage Current vs. Voltage

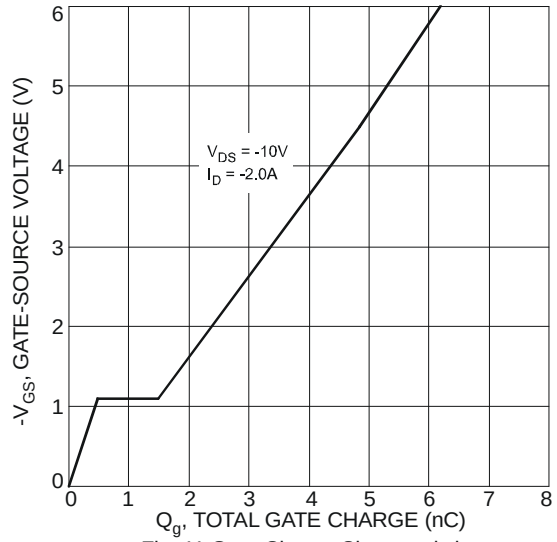


Fig. 11 Gate-Charge Characteristics

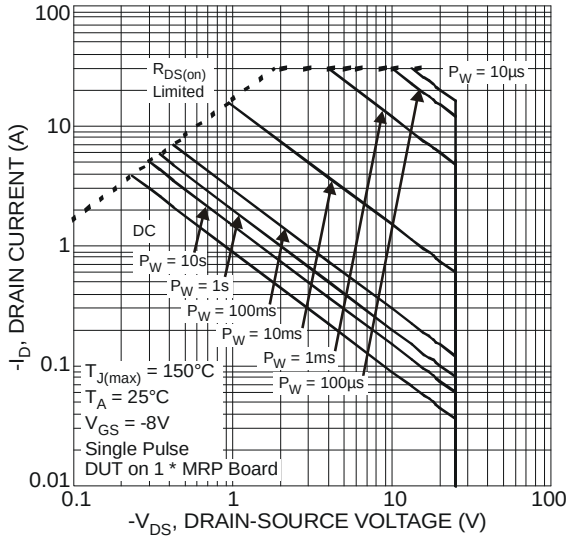


Fig. 12 SOA, Safe Operation Area

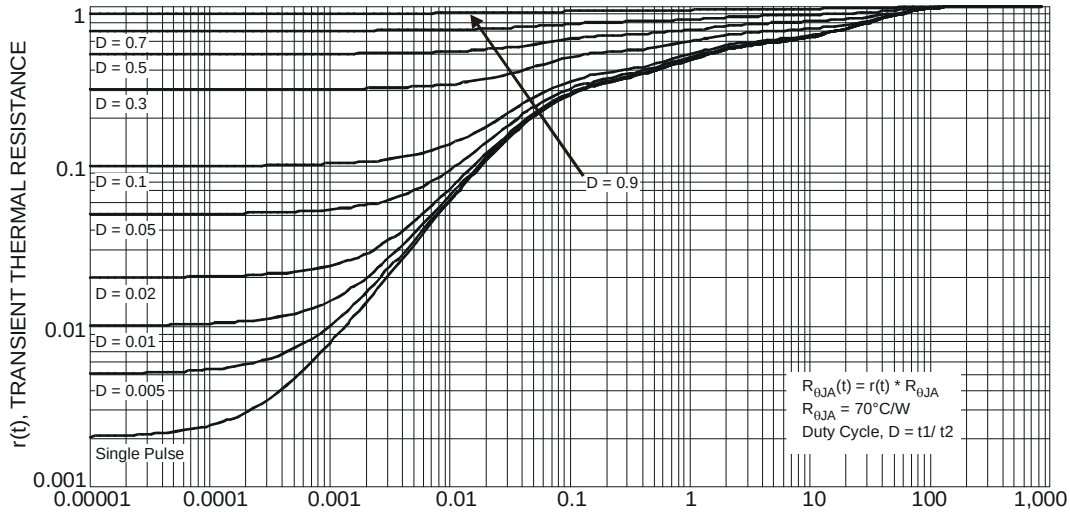
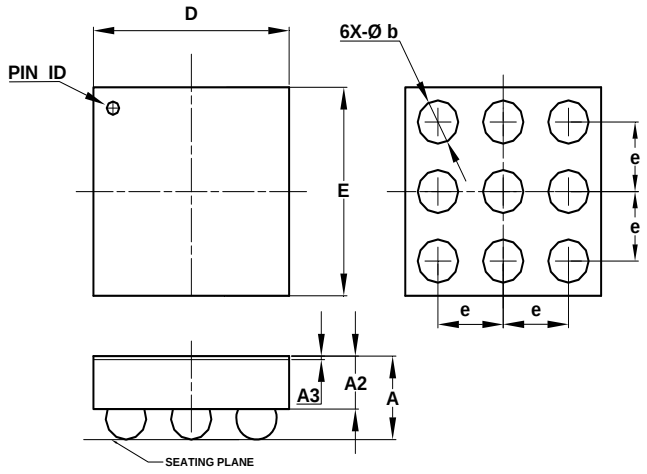


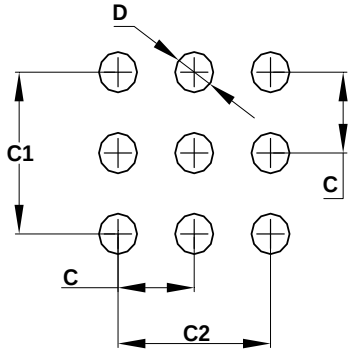
Fig. 13 Transient Thermal Resistance

Package Outline Dimensions



U-WLB1515-9			
Dim	**Min**	**Max**	**Typ**
A	-	0.62	-
A2	-	0.36	0.36
A3	0.020	0.030	0.025
b	0.27	0.37	0.32
D	1.47	1.51	1.49
E	1.47	1.51	1.49
e	-	-	0.50
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

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